AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (original): An erroneous operation preventing circuit of an electrically rewritable non-volatile memory device for setting one or more operational modes of a plurality of operational modes including at least a first reading mode of reading out data from a memory array, a programming mode of writing data to the memory array, an erasing mode of erasing data from the memory array and a second reading mode of reading out data not stored in the memory array, in accordance with an input control command, and for performing a predetermined process in the set operational modes, the circuit comprising:

an operational mode enforcing circuit for setting the first reading mode regardless of the input control command, in a data protection status where the programming mode and the erasing mode are inhibited from being set in accordance with a control signal for protecting predetermined data.

Claim 2 (original): The erroneous operation preventing circuit of a non-volatile memory device according to claim 1, further comprising a data protection area specifying unit for specifying a data protection area such that the data protection status would be valid only in the specified data protection area in the memory array,

wherein the operational mode enforcing circuit sets the first reading mode regardless of the input control command, when the data protection area is specified by means of an input address in the data protection status.

Claim 3 (original): The erroneous operation preventing circuit of a non-volatile memory device according to claim 1, wherein the operational mode enforcing circuit allows the operational mode to

be set in accordance with the input control command, in a status where the programming mode and the erasing mode are not inhibited from being set in accordance with the control signal.

Claim 4 (original): The erroneous operation preventing circuit of a non-volatile memory device according to any one of claim 1, wherein the control signal includes one or more of a control signal specified for data protection, a data-writing high voltage input signal, a data-erasing high voltage input signal and a data-writing/erasing high voltage input signal provided independently.

Claim 5 (original): An erroneous operation preventing circuit of an electrically rewritable non-volatile memory device for setting one or more operational modes of a plurality of operational modes including at least a first reading mode of reading out data from a memory array, a programming mode of writing data to the memory array, an erasing mode of erasing data from the memory array and a second reading mode of reading out data not stored in the memory array, in accordance with an input control command, and for performing a predetermined process in the set operational modes, the circuit comprising:

an operational mode enforcing circuit for enforcedly setting an inner level of a control command input circuit to an inner level corresponding to the first reading mode regardless of an input level of the control command, in a data protection status where the programming mode and the erasing mode are inhibited from being set in accordance with a control signal for protecting predetermined data.

Claim 6 (original): The erroneous operation preventing circuit of a non-volatile memory device according to claim 5, further comprising a data protection area specifying unit for specifying a data protection area such that the data protection status would be valid only in the specified data protection area in the memory array,

wherein the operational mode enforcing circuit enforcedly sets the inner level of the control command input circuit to the inner level corresponding to the first reading mode regardless of the input level of the control command, when the data protection area is specified by means of an input address in the data protection status.

Claim 7 (original): The erroneous operation preventing circuit of a non-volatile memory device according to claim 5, wherein the operational mode enforcing circuit sets the inner level of the control command input circuit to the inner level corresponding to the input level of the control command, in a status where the programming mode and the erasing mode are not inhibited from being set in accordance with the control signal.

Claim 8 (original): The erroneous operation preventing circuit of a non-volatile memory device according to any one of claim 5, wherein the control signal includes one or more of a control signal specified for data protection, a data-writing high voltage input signal, a data-erasing high voltage input signal and a data-writing/erasing high voltage input signal provided independently.